A 94GHz low power UWB LNA for passive radiometer

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Abstract— **This paper presents a low power millimeter- wave low noise amplifier (LNA) for the passive radiometer systems with monolithic transformer feedback to neutralize gate-drain overlap capacitance of a MOSFET. The LNA adopts four-stage common source topology implemented in general purpose 65nm CMOS technology. Designed for central frequency of 94GHz, LNA achieves maximum simulated power gain of 14.5dB with 3dB bandwidth of 16.4GHz. Minimum noise figure (NF) is 5.2dB at 94GHz. LNA occupies a compact core area of 320µm×130µm while dissipating only 16mW at 1.2V.**

Keywords - low noise amplifier (LNA), millimeter-wave imaging, millimeter-wave integrated circuits, monolithic transformer/inductor, neutralization, passive radiometers.

I. INTRODUCTION

HIGH-RATE communication links, automotive radars and imaging systems, lead to the use of millimeter-wave frequencies. For radar and imaging systems, higher frequency signals offer the benefit of better angular and spacial resolution. Also, higher frequencies improve reflection or transmission profiles for object detection and imaging. Millimeter-wave passive radiometers are interesting due to their low power consumption and their simple architecture when compared to their active counterparts [1]. Unfortunately, these benefits come at a price of reduced signal to noise ratio (SNR). These systems require large system bandwidth and high front-end gain while producing minimum amount of output noise to achieve sufficient sensitivity.

For the high performance millimeter-wave imaging receivers, it is extremely important to achieve a low minimum resolvable temperature given as [2]:

$$\Delta T_M = T_S \sqrt{\frac{1}{B\tau} + \left(\frac{\Delta G}{G}\right)^2} \quad (1)$$

where T_S is the system noise temperature, B is RF front-end bandwidth, τ is the receiver's integration time, ΔG is the effective value of the imaging receiver gain variation, and G is the overall gain of the receiver front-end.

As the first block in receiver, the noise performance of LNA is essential for the sensitivity of the whole system. In radiometer circuits LNA should have high gain to suppress noise contribution of following stages such as detector circuit. In other words, LNA for radiometer systems should simultaneously employ low noise figure, high gain and high bandwidth as shown in equation (1) to keep resolvable temperature as low as possible. Also, power consumption should be kept at minimum in order to maintain power budget benefit compared to active radiometers. However, as frequency increase, amplifier designers can no longer neglect the effect of metal-oxide-semiconductor field-effect-transistors (MOSFET) gate-drain overlap capacitance C_{gd} on performance since it is comparable with gate-source capacitance in deep-submicron technologies. In mm-wave frequency C_{gd} makes it difficult to achieve high gain and low noise figure while maintaining stability in higher frequency range [3].

Various LNA for the 100GHZ frequency range have been presented in III-V materials SiGe HBT [4], [5] and InP HEMT [6], [7]. While III-V materials provide higher performances, a silicon implementation is desirable for its lower integration cost, high yield, continuous scaling and potential of full integration with digital circuits.

Four-stage LNA demonstrated in this paper employ reactive negative feedback through on-chip transformer to neutralize gate-drain overlap capacitance C_{gd} while keeping DC voltage drain-source to be equal to power supply voltage thus not degrading maximum f_T of MOSFET.

Paper is organized as follows; second section presents brief overview of unilateralization and neutralization of gate-drain capacitance and introduction to voltage-voltage transformer feedback. Third section presents LNA topology and its design. Fourth section contains simulation results and final section V finalizes with conclusion.

II. NEUTRALIZATION AND UNILATERALIZATION

Miller capacitance C_{gd} adds a noninverting signal path which reduces gain and feedback path through C_{gd} reduces output to input isolation which can lead to instability of the amplifier. Gate-drain capacitance also reduces f_T of the transistor (2) and its effect in a common source configuration on input capacitance is multiplied by the Miller effect (3).

$$f_T = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)} \tag{2}$$

$$C_{eq} = C_{gd}\left(1 + A_v\right) \tag{3}$$

Standard technique used to mitigate gate-drain capacitance is to implement unilateralization (unilateralization decrease reverse signal flow and thus, coupling between output and input port of the amplifier) by cascoding common-source and common-gate stage. While cascode topology with inductive degeneration is commonly used in RF design because it improves reverse isolation and it is unconditionally stable at the operating frequency making the design more robust, cascode configuration is not suitable for low voltage applications because it requires additional voltage headroom. Also, at mm-wave frequencies common-source amplifier has better performance than the cascode amplifier due to the low gain of the common-source (CS) transistor and high noise of the common-gate (CG) transistor. The noise contribution of the CG transistor increases, which makes cascade topology not the best choice for low noise applications at mm-wave frequencies although cascode stage have few dB larger gain than CS stage [8].

Second technique group to mitigate gate-drain capacitance are called neutralization. This technique cancels signal flow through C_{gd} by adding additional signal path, so that the net signal flow through C_{gd} and the additional path is zero. This increase forward gain and reverse isolation for a given power consumption but it does not necessarily reduce effect of C_{gd} on input capacitance. One of the neutralization techniques for the differential amplifier is given in [9]. This topology suitable for differential topologies uses cross-coupled capacitors C_N to cancel the signal flow through C_{gd}. Unfortunately, this topology is not suitable for single ended amplifiers and also requires precise matching of C_N and C_{gd}. Signal flowing through C_N is actually positive feedback that can cause instability if C_N is not equal to C_{gd} [10].

In this paper we used topology shown in Fig. 1 called voltage-voltage transformer feedback LNA for improving reverse isolation and stability [11].

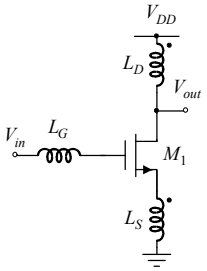

Figure 1. Voltage-voltage transformator feedback topology.

Benefit of this topology compared to the cascode topology is that this topology does not require additional voltage headroom for cascoded device and it can be used in low voltage applications. Another important advantage of this topology is that L_S and L_D inductors are coupled and they occupy less space than standard CS topology.

Condition to achieve frequency independent unilateralization by making Z_{12} (4) of the circuit equal to zero is given by equation (6),

$$Z_{12} = \frac{sL_D\left(C_{gd} - \frac{k_c}{n}C_{gs}\right) + \frac{s^2\left(1-k_c^2\right)}{n^2}C_{gd}L_D^2\left(g_m + sC_{gs}\right)}{s\left(C_{gs}+C_{gd}\right) + \frac{s^2C_{gd}L_D}{n^2}\left(1+2k_cn+n^2\right)\left(g_m+sC_{gs}\right)} \tag{4}$$

$$k_c = \frac{M}{\sqrt{L_S L_D}}, n = \sqrt{\frac{L_D}{L_S}} \tag{5}$$

$$k_c = 1, n = C_{gs}/C_{gd} \tag{6}$$

where coupling factor k_C and turn ratio n of the transformer are defined as in equations (5). The condition of frequency independent unilateralization is satisfied only if coupling factor k_C is equal to one and if transformation ratio is equal to the ratio of C_{gs} and C_{gd}. If condition (6) is not satisfied it is not possible to obtain frequency independent unilateralization. In case of unilateralization which is achieved by meeting conditions (6) input impedance is given by equation:

$$Z_{11} = R_G + j\omega L_G + \frac{1}{j\omega\left(C_{gs}+C_{gd}\right)} \tag{7}$$

From equation (7) if L_G resonates with (C_{gs} + C_{gd}) the Z-parameters derived from Fig. 1 are as follows:

$$\begin{aligned} Z_{11} &= R_G, \\ Z_{12} &= 0, \\ Z_{21} &= \frac{-g_mL_D}{1-\omega^2C_{gd}L_D\left(C_{gs}+C_{gd}\right)+j\omega\frac{g_mC_{gd}L_D}{C_{gs}}\left(C_{gs}+C_{gd}\right)}, \\ Z_{22} &= \frac{j\omega C_{gs}L_D}{1-\omega^2C_{gd}L_D\left(C_{gs}+C_{gd}\right)+j\omega\frac{g_mC_{gd}L_D}{C_{gs}}\left(C_{gs}+C_{gd}\right)} \end{aligned} \tag{8}$$

and transducer gain when the condition (6) is satisfied is:

$$\begin{aligned} G_T = {} & \frac{j\omega g_m^2L_D^2n^2\left(1+n\right)}{C_{gd}\left(n^2+j\omega g_mL_D\left(1+n\right)-\omega^2L_Dn\left(C_{gs}+C_{gd}\right)\right)} \\ & \times\frac{1}{n^2R_L+j\omega L_D\left(n^2+g_mR_L\left(1+n\right)\right)-\omega^2nL_DR_L\left(C_{gs}+C_{gd}\right)} \\ & \times\frac{1}{1+j\omega\left(C_{gs}+C_{gd}\right)\left(R_G+R_S\right)-\omega^2L_G^2\left(C_{gs}+C_{gd}\right)} \end{aligned} \tag{9}$$

III. LNA DESIGN

A four stage common source circuit topology with voltage-voltage transformer feedback discussed in previous section has been designed, as shown in Fig. 2, in 65nm general purpose bulk CMOS technology with 9 metal layers. The thickness of metal 9 and metal 8 are 3.4μm and 0.9μm respectively, metal 7 to metal 2 are 0.22μm thick and metal 1 thickness is 0.18μm.

The main objectives, beside from stability and reverse isolation discussed in previous section, are low noise figure and high gain. Both are function of the transistor biasing and width, passives choices and source impedance. Transducer power gain of the LNA after unilateralization is given by expression (9), where R_L is load resistance (not shown in Figure 2). From the last term in (9) we can clearly see that if L_G resonates with (C_{gs} + C_{gd}) transducer gain is maximized. This condition is identical to the one required for canceling imaginary part of input impedance.

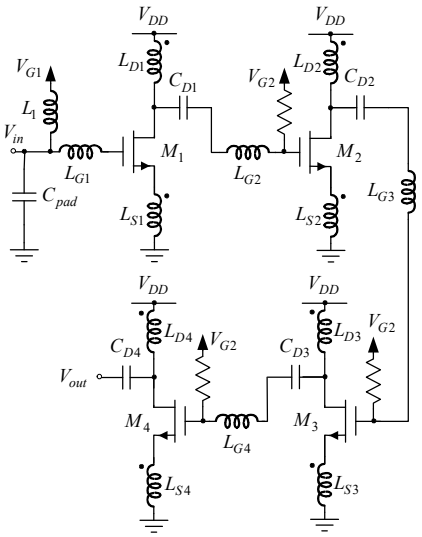

Figure 2. Designed four-stage LNA.

Four stages are cascaded together, as shown in Fig. 2, to achieve acceptable gain compared to the state of the art low noise amplifiers. The layout of the core of the LNA is shown in Fig. 3. Input matching network is shown on the upper left and it consists of two inductors L_1 and L_{G1} while the output of the LNA is located on the right. Four stages are cascaded using DC-blocking capacitors and matching inductors L_{G2}, L_{G3} and L_{G4}. All the RF interconnects longer then 15μm are simulated in 3D electromagnetic simulator to account for their parasitic inductances, their parasitic capacitances and loss. The rest of the layout is simulated after RC extraction. The parasitic inductances in signal path are included either in inter-stage inductors (L_{G2}, L_{G3}, L_{G4}), transformers or input matching network.

Transistor widths for all four stages are 15μm with finger width of 1μm. Transistor M_1 is biased for minimum noise figure while transistors M_2 through M_4 are biased for maximum f_T [12]. Special attention is paid to keeping the interstage connections as short as possible to avoid increasing the parasitic capacitances.

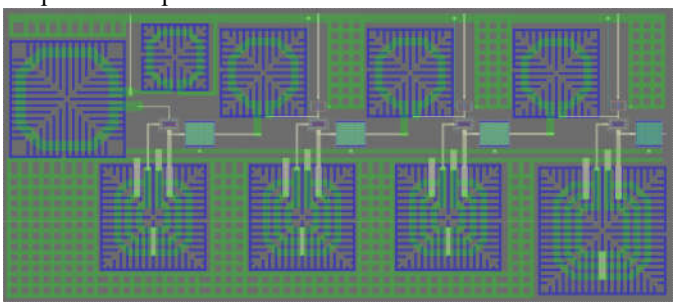

Figure 3. Layout of the designed LNA.

Inter-stage inductors used for cascading amplifier stages have the same value of approximately 60pH at 94GHz. Series input matching inductor (L_{G1}) and shunt inductor (L_1) are approximately 70pH and 35pH respectively. All inductor are realized in metal 9 which is thickest and have lowest parasitic capacitance. Polysilicon patterned shield is placed underneath all inductors to reduce parasitic coupling to the substrate.

The used transformers and inductors are designed using EM simulations with 3D electromagnetic simulator. The layout of the transformer is shown in Fig. 4. Transformer utilizes octagonal structure with primary turn (L_S) consisting of inner and outer turn connected in parallel while middle turn represents secondary turn (L_D). Transformer is realized in metal 9 for lowest parasitics and highest Q factor. The widths of the metal lines are chosen to be 3μm as compromise between Q factor and self-resonant frequency of the transformer.

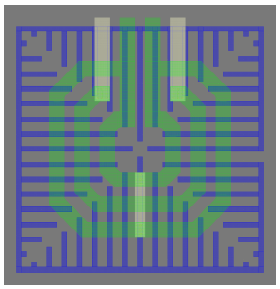

Figure 4. Transformator layout.

While a coupling factor of k_C=1 is needed for satisfying condition (6) for frequency independent unilateralization, best we could do was 0.5 while maintaining self-resonant frequency of transformer higher than operating frequency of the amplifier. The simulated Q factors for both primary and secondary turn are higher than 10 at the frequency range of interest. For smaller transformer used in first three stages of the LNA primary (L_S) and secondary (L_D) turn inductances are approximately 20pH and 50pH respectively. For larger transformer used in last stage of the LNA primary and secondary turn inductances values are 30pH and 70pH respectively. As well as in the inductor, polysilicon patterned shield is placed underneath transformer to reduce parasitic coupling to the substrate.

Input and output of the LNA are matched to 50Ω. Input matching network consists of inductors L_1 and L_{G1}, pad capacitance C_{pad} and input capacitance of first stage of the LNA. Output is matched using L_{D4} of the fourth stage transformer and output parasitic capacitance.

IV. Simulation Results

Corner analysis of the noise figure and transducer gain of the designed LNA are shown in Fig. 5. Nominal simulated noise figure is 5.2dB at 94GHz. Maximum transducer power gain of the LNA for nominal parameters is 14.5dB at 91GHz with 3dB bandwidth of 16.4GHz (83.9GHz – 100.3GHz). Worst case minimum noise figure and maximum transducer power gain are 6.2dB and 13.26dB respectably for slow SS models at 80°C. Noise figure and power gain in best case scenario (fast FF models at 0°C) are 4.6dB and 15.2dB respectably.

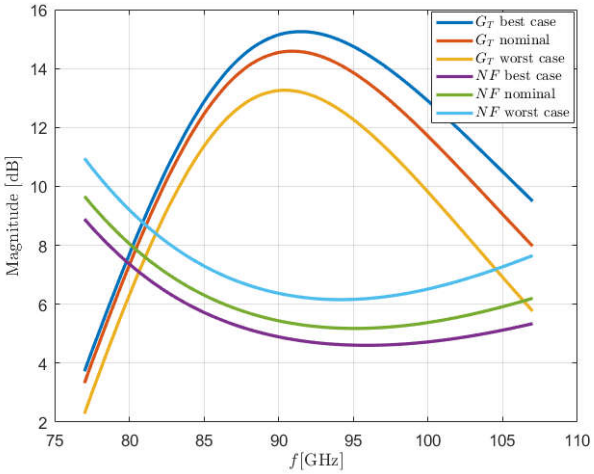

Figure 5. Corner analysis for transducer gain and noise figure.

Corner simulations for input and output return loss (S_{11} and S_{22}) are shown in Fig. 6.

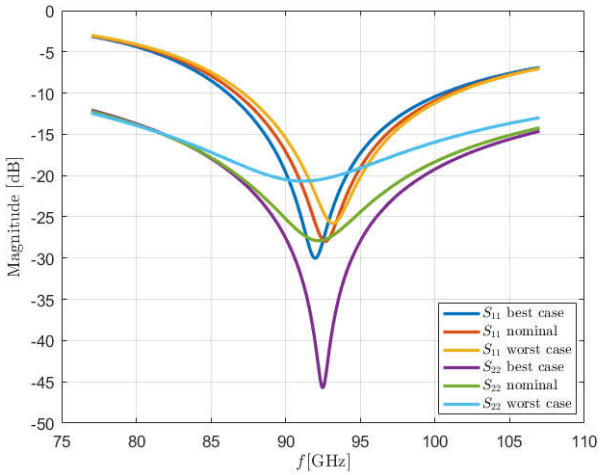

Figure 6. Corner analysis for input and output return loss (S_{11} and S_{22}).

From corner analysis, input return loss S_{11} is lower then -10dB in frequency range from 86.7GHz to 100.5GHz while output return loss S_{22} is better then -15dB within the frequency range of interest. Output to input isolation S_{12} is shown in Fig. 7 and it is better then -85dB even in the worst case.

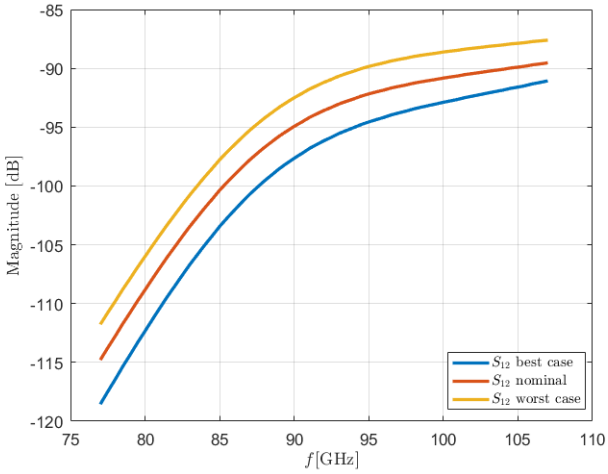

Figure 7. Reverse isolation S_{12} corner analysis.

Input referred 1dB compression point P_{1dB} for nominal parameters is equal to -13.5dBm while the input referred third order intercept point IIP3 is equal to -3.5dBm. All simulations are performed using Cadence simulation tools.

With a power supply of 1.2V power consumption of LNA is only 16mW. Simulated performance of this LNA shows promising features of the designed circuit. Designed LNA is compared to other state-of-the-art LNAs in Table I.

TABLE I. Performance Summary and Comparison with State-of-the-art MM-wave Wideband LNAs.

	[9]*	[13]	[14]	[15]	This work*
Technology	65nm LP CMOS	65nm CMOS	65nm CMOS	65nm CMOS	65nm GP CMOS
f_c(GHz)	107	100	104	86	92.5
Gain(dB)	10.2	13	16.7	15	14.5
NF(dB)	8	7.5	7.2	7	5.2
Topology	2 stage CS	3 stage CS	5 stage Cascode	5stage CS	4 stage CS
3dB BW (GHz)	16	21	21.5	12	16.4
P_{DC} (mW)	28.2	86	48.6	42	16

* EM simulated results

V. Conclusion

In this paper, a four-stage LNA operating in 94GHz band is designed using 65nm general purpose CMOS PDK. The LNA employs voltage-voltage transformer feedback common source LNA for gate-drain capacitance neutralization in order

to reduce input to output isolation and improve stability of the amplifier. With 50Ω input and output load LNA achieves 14.5dB transducer gain with wide bandwidth of 16.4GHz. Input referred intercept point IIP3 and input referred 1dB compression point are -3.5dBm and -13.5dBm respectively. Minimum noise figure of the LNA is equal to 5.2dB at 94GHz. LNA consumes less than 13.2mA from the power supply of 1.2V resulting in low power dissipation of only 16mW.

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