Sensor Networks Energy Efficiency in Subthreshold Voltage Domain

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Abstract— **Energy efficient design is the most common approach when designing electronic systems, whether that is a battery for mobile device, thermal dissipation of highly efficient processors or extremely low power wireless sensor applications. Economic impacts and increasing environmental awareness are setting new conditions in the design of electronic systems. In addition, the leading factor in the choice of new manufacturing strategies of today is energy efficiency. This paper offers an overview of the recent research in sensor networks energy efficiency in the subthreshold supply voltage domain.**

Keywords - Energy efficiency; Subthreshold voltage; Sensor networks

I. INTRODUCTION

Energy is the main limiting factor for designers of integrated circuits. As the number of transistors on a chip grows as presented by Moore's law, from the beginning of the seventies of the previous century, it is necessary to adjust power use and functionality of the design. Moore's law describes the increasing number of transistors on a chip over time as follows: "The number of transistors that can be placed on a chip at the best price doubles roughly every two years." Such progress had resulted in the rapid development of computer applications which have applications in healthcare, education, communications, and security. However, the use of Moore's law as a measure of progress, have to be taken with caution since we have to be aware that increasing the number of transistors we do not have proportional increase in energy efficiency. Survival of the semiconductor industry largely depends on the development of energy efficient solutions in terms of energy dissipation.

In the first period of the development of electronics, the basic elements in electronic circuits were vacuum or gas tubes, then the logic circuits with NMOS transistors were used because the CMOS technology was too complex at the time to be economically viable for chips with a high degree of integration. With the improvement of technological processes, CMOS technology fully replaced NMOS technology at all levels of integration for both analog and digital applications. The main motive behind changes in production technologies and technological processes is to improve the energy consumption. Today, however, there is no clear successor to CMOS technology. Existing alternatives are far from commercial viability, and none of the current and potential alternative technologies provide an economic justification for rejecting the major investments made in CMOS-based infrastructure. Therefore, energy efficiency solutions should be based on the improvement of existing devices, including their design and architecture, rather than relying on radical new technologies that could be widely applied in the near future.

The most common limiting factor when designing electronic systems is energy, whether that is a battery for mobile device, thermal dissipation of highly efficient processors or extremely low power wireless sensor applications. In addition, economic impacts, and increasing environmental awareness, are setting new requirements in the design of electronic systems. The leading factor in the choice of new manufacturing strategies of today is energy efficiency. Optimization of devices, circuits and architectures is essential within the growing energy constraints. Optimization should be implemented on a wide scale, thus including semiconductor process technology, circuit design techniques, systems architecture, platform configuration and design methodology.

II. VLSI TECHNOLOGY SCALING

VLSI technology scaling has continued over the past several decades and provides effective, affordable devices that enrich lives and that we are fully accustomed to. Although the technology scaling continues, doubling the number of transistors in each generation, scaling of the supply voltage does not necessarily reduce the energy per operation, so that all existing transistors can be used.

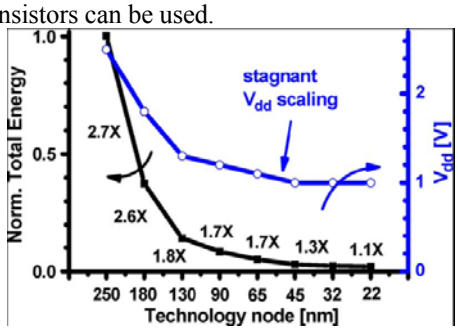

Figure 1. Technology scaling trends of supply voltage and energy

Scaling down the supply voltage is an effective way of reducing energy since it brings quadratic saving in dynamic energy consumption and linear reduction in leakage power [1] but starting around the 65 nm technology node, device scaling no longer delivers the energy gains that drove the semiconductor growth of the past several decades. This is shown in Fig. 1. [2]. Therefore, the next challenge that needs to be faced is energy efficiency, but not just thinking low power, but rather still providing the data flow with lower energy consumption. Energy per operation will have to be reduced by an order of magnitude. Working with supply voltage circuits that are near the threshold voltage of the transistors provide greater energy efficiency. As the supply voltage is scaled down into the near-threshold region, between 400 and 700 mV, the energy per opertion is considerably reduced and the delay is reduced as well. Operating in the near threshold region offers much of the energy savings in comparison to subthreshold operation while at the same time offers better performance and variability characteristics. This makes operating in this region applicable to a broad range of power constrained computing segments including energy constrained sensing platforms. Authors in [3] explore the barriers to the adoption of NTC and describe current work aimed at overcoming these obstacles in the circuit design space. As the voltage is scaled down even further, delay increases exponentially, and the total energy per cycle increases because energy due to leakage becomes the dominant part [4]. Subthreshold circuits use a supply voltage that is below the threshold voltage of the transistors. By the conventional definition the transistors are "off", but the change in transistor 'gate to source' voltage produces a difference in subthreshold conduction current that allows static digital circuits to operate reliably although much slower than they would be at higher voltage. The lower speeds are still more than sufficient for many body sensor networks (BSN) operations that are in the range of up to 10's of MHz. Both 'on' and 'off' currents fluctuate exponentially with supply voltage in the subthreshold, but there is a substantial difference between them to enable proper functionality of the digital gates [5]. Considering that the relationship between energy and supply voltage is quadratic, the main advantage of operating in the subthreshold region is reduction in energy consumption of over 10 times compared to traditional circuit implementations. For this reason, subthreshold operation will play an important role in custom hardware for BSNs. Hence, energy constrained applications such as wireless sensor nodes, RFID tags, or implants are dominated by the need to minimize energy consumption. Speed is a secondary consideration for this class of applications, so subthreshold circuits offer a good solution. Authors in [6] are applying subthreshold and near-threshold techniques to chip multi-processors where they present an architecture where several slower cores are clustered together with a shared faster L1 cache that is optimal for energy efficiency, because processor cores and memory operate best at different supply and threshold voltages.

A circuit sensitive to changes in voltage will cease to function when supply voltage is approaching the threshold voltage of the transistors. Circuits must be designed in such a way to take into account the additional effects that would occur when lowering the value of the supply voltage. For example, SRAM is an important component of many integrated circuits and it can contribute to a large portion of active power consumption as well as energy leakage consumption. In this work we will focus on the overview of techniques necessary for designing reliable operation of the system for supply voltages that are below the threshold voltage of transistors.

III. SENSOR NETWORKS

Wireless sensor networks have applications in medicine, military, inventory management, structural and environmental monitoring, and have become a platform that changes how we interact with the physical world. We can benefit from low-power wireless nodes that communicate data collected via a variety of sensors. Currently, wireless sensor networks solutions offer un-optimized energy consumption of these systems and their effective lifetime is limited. Ideally, researchers would like to deeply embed wireless sensor network nodes in the physical world, relying on energy scavenged from the ambient environment [7]. There is a large market for sensor networks and wearable computers, amongst others, where circuit speed is a secondary design goal and the design requires extreme low power circuits.

On the other hand, reconfigurable designs are becoming more and more popular as a means of implementing digital designs due to their increasing speeds in connection with technology progress [8]. Besides this, reconfigurable designs are becoming viable for larger and larger sets of applications. Application Specific Integrated Circuits (ASICs) are becoming more expensive to design and implement, due to extreme fabrication costs in the VLSI industry [9]. All of this contributes to the fact that reconfigurable designs are becoming an implementation choice of digital designs.

A new procedure for creating VLSI circuit designs that enables considerably lowered power consumption in these circuits has been developed by researchers at Texas A&M University [9]. Their invention is based on the use of subthreshold currents that have been explored by researchers in the past, but the exponential dependence of the delay of the subthreshold circuit on temperature, processing, and operating voltage (PVT) variations has created numerous limitations on their broader usage. The dynamic body biasing approach is the key to the design and ensures that the speed of the reconfigurable design is constant, regardless of the PVT conditions. The problems in the variance of device operating points caused by temperature changes, operating voltage drift, and manufacturing irregularities which have prevented practical applications of subthreshold circuits have been addressed in this research. This novel approach is intended to enable the design of battery-less, ambient light powered reconfigurable VLSI circuits.

Advantages [9]:

- No known technique achieves the reconfigurability and extreme low power feature that is addressed by this design.

- Provides the ability to allow digital designs to be realized with extreme low power consumptions (100X to 500X lower than previous approaches).
- Allows designers to realize reconfigurable designs, which dramatically reduce Non-Recurring Engineering (NRE) costs associated with implementing digital designs.
- Applications include situations where the circuit can operate very slowly and it is desirable to operate with power consumption two orders of magnitude below current low power circuits. Examples would be hearing aids and smart clothing.

IV. MINIMIZING ENERGY CONSUMPTION WITHIN SENSOR NETWORKS

Energy consumption in a random sensor node is in general attributed to sensing, communication and computation energy. Sensing energy is dissipated in order to activate sensing circuitry and gather data from the environment. The magnitude of this energy depends on the task that is assigned to the sensor. Different sensors require different levels of energy during operation. Communication energy is consumed by the node while sending or forwarding data packets to the base station. It includes transmission energy and receiving energy. Operation of the sensor node includes the activation of the sensor's processor or microcontroller. Moreover, whenever data aggregation is carried out, additional computation must be performed. Compared to the previous items, computation energy is usually relatively low.

Various approaches have been proposed to reduce energy consumption due to the computation and communication, considering sensor requirements differ based on the application. The authors in [8] elaborate on general strategies for designing energy efficient hardware, focusing on the tradeoffs of computation versus communication, flexibility versus efficiency, and data fidelity versus energy. The low power of an arbitrary sensor node is one of the most important aspects of sensor network energy optimization. Basically, if the node itself is not energy efficient, higher layer optimization cannot decrease the energy consumption due to the fact that sensor node hardware consumes energy.

Power consumption in circuit design has been an interesting topic in the past as well as present, and has encouraged a significant investigation in the domain of design optimization for minimizing energy or power for a given performance constraint. Some of the new circuit techniques are supporting a pursuit to reduce power consumption. Amongst others, it has been done by removing clocking overhead by asynchronous circuits and also by exchange of performance for lower power consumption as in using supply voltages that are below threshold voltage. Considering an increase in leakage current due to transistor shrinking, some systems have architecture support for circuits that power off the supply voltage of unused blocks and that way reduce leakage current. Thus, systems based on the circuit techniques employed to reduce total energy consumption can be categorized by [7] as:

- Subthreshold operation - By using a power supply less than the threshold voltage, systems such as the Subliminal processor [10] are able to trade off performance for reduced active power consumption. Subthreshold circuits have drawn a strong interest in recent ultralow power research.
- Asynchronous Circuits - Processors such as SNAP eliminate clock power by relying on asynchronous circuits.
- Power Supply Gating - To address increasing leakage current, systems employ transistors that switch the power supplies of unused blocks.

The subthreshold approach has been demonstrated to be effective in designing circuits with limited energy supply, and therefore is receiving continuing attention from researchers interested in ultra-low power design in particular wireless sensor networks and ubiquitous computing. The key to subthreshold design is the recent work reported by several authors which has already established the importance of leakage current contribution to the total power in subthreshold designs [11].

Applications in their development such as distributed sensor networks or medical applications put performance concern second to low energy consumption, with the subsequent objective of harvesting energy from the environment [12]. This paper presents the first HDL-based modeling approach that links the system's energy generation and consumption with its analog parts and digital processes. Subthreshold operation is ideal for such applications because it allows minimum energy operation for low-performance situations. Researchers in [13] have examined minimum energy operation for subthreshold circuits. Authors have shown that the minimum energy point depends on the technology, the characteristics of the design, and on operating conditions such as temperature, duty cycle, and workload, and concluded that minimum-sized devices are theoretically optimal for minimizing power. Even if the minimum energy point for a certain process corner or unusual circuit occurs at a supply voltage where minimum sized devices cannot function, the shallow nature of the optimum prevents up-sizing to reduce the minimum possible operating voltage from being worthwhile. In [14] task completion latency was maintained while the limit of voltage scaling together with task parallelization was investigated. The near threshold region for maximum energy efficiency is roughly 200mV-400mV above threshold voltage for most applications and this trend held for the six technology nodes that were examined.

Highly integrated sensor network platforms would combine MEMS sensing capabilities with digital processing and storage hardware, a low power radio, and an on-chip battery in a volume on the order of 1 mm^3. The design of energy-efficient data processing and storage elements is therefore of crucial importance. In [11], the researchers' investigation determines that the architectural decisions on micro levels in the subthreshold system differ significantly from that in conventional superthreshold mode. Authors propose a new general-purpose sensor processor architecture,

which they call the Subliminal Processor, which is presented as a highly efficient subthreshold microprocessor targeting sensor applications. Its optimization is realized across different design stages including ISA definition, microarchitecture evaluation, and circuit and implementation optimization. On the circuit side, subthreshold operation is known to exhibit an optimal energy point (V_{min}). However, delay also becomes more sensitive to process variation and can reduce the energy scaling gain. Detailed analysis has been conducted on how supply voltage and operating frequency impact energy efficiency statistically. With careful library cell selection and robust static RAM design, the Subliminal Processor operates correctly down to 200 mV in a 0.13-µm technology, which is sufficiently low to operate at V_{min}. Silicon measurements of the Subliminal Processor show a maximum energy efficiency of 2.6 pJ/instruction at 360 mV supply voltage and 833 kHz operating frequency. Finally, the variation in frequency and V_{min} across dies is examined to verify their analysis of adaptive tuning of the clock frequency and V_{min} for optimal energy efficiency [11].

Subthreshold circuits are mostly applied to operating settings that are strictly constrained, whether that constraint is energy or power. For example, wearable body sensors or wireless sensor requirements are to be small and long lasting, but they do not require high operating frequencies. These types of energy-constrained applications are perfect for subthreshold circuits, which can provide digital signal processing up to several tens of megahertz at extremely low energy per operation. For example, in [15] authors demonstrated a 0.13-µm CMOS mixed-signal system on chip that implements an electrocardiogram. The system on chip includes an analog front end, AD converter and a subthreshold microprocessor. The processor consumes only 1.5 pJ at 280 mV (700 nW), and it is used for signal processing and for controlling of the analog circuitry. The chip is designed for monitoring cardiac arrhythmias in patients, whose presence can be identified by abnormalities in the heart rate, making full transmission only necessary when actual arrhythmic events occur. It is possible to reduce the wireless data rate by more than 500 times by extracting the heart rate interval on chip and reducing the use of a radio transmission. The heart rate algorithm can continue to operate accurately even when the analog components operate at lower voltages to save power. The work in [16] introduces the use of compressed sensing algorithms for data compression in wireless sensors to address the energy and bandwidth constraints common to wireless sensor nodes. The circuit architecture is implemented in a 90 nm CMOS process and the analysis shows that digital implementation is significantly more energy efficient for the wireless sensor space where signals require high gain and medium to high resolutions. Authors in [17] brought together papers on approaches spanning circuits, architectures, algorithms, and system design that demonstrate promising solutions to emerging critical problems in BSNs. Some of them presents a 0.1 V dosimeter using FGRADFETs on a 0.8-µm CMOS chip for On-body Radiation Dose Measurements. This sensor consumes only 1 µW during readout and exhibits increased sensitivity, making it well suited for power limited BSNs [18]. Article [19] presents a 2.4-GHz receiver architecture that has been tailored specifically for the channel properties of BSNs. Measured BSN channel data and measured silicon chip performance is presented.

In [20], authors address three key points. In the first section, they show how subthreshold operation can be used to achieve energy optimization. They then highlight one of the primary problems facing subthreshold circuit designers: variability. In the final section, they relate the topics of the first two sections to measurements of a real subthreshold design. The chip under test is a subthreshold sensor network processor with an 8-bit CISC architecture and a 2-kbit memory. The processor, fabricated in a 130 nm technology, occupies an area of 85,022 μm^2. The energy minimum of 2.6 pJ per instruction occurs at V_{dd}=400 mV, which is significantly higher than the minimum energy voltage observed for the inverter chain observed in the same paper. Recall that V_{min} tends to be higher for circuits with lower switching activity. The memory, which has a very low switching activity compared to typical logic, accounts for 65% of the total transistor area and is largely responsible for the higher V_{min}. Due to higher leakage current in SRAMs compared to logic, memories reach their optimal energy/delay trade-off at higher voltages than cores: 870mV for SRAM and 670mV for logic in 130nm technology [21]. Hence, SRAMs ideally operate at a higher voltage than cores, improving their speed.

The enormous amount of work relating to sensor processor design has been focused on supply voltages that are substantially above threshold voltage, resulting in higher energy consumption and delivering performance that is not necessarily needed. The processor presented in [22] represents new level of energy efficiency for sensor network processors, considering that the power consumed in the active state is usually lower than the idle power consumption of other sensor processors. This second generation solution was nearly three times more efficient than the previous one and almost 25 times more efficient than most designs found in the literature in that period.

V. CONCLUSION

Scaling of process technologies has made power management a significant concern for circuit designers. For progressing low power applications such as distributed sensor networks or medical applications, low energy operation is the primary concern, as well as collecting energy from the environment. Lowering the circuit supply voltage is a recognized approach for reducing energy. Designing hardware for wireless sensor networks requires a universal approach looking at all areas of the design space. Resolving the issue of reducing the system functionality error, which occurs because of increased sensitivity to process, voltage, and temperature variations, should be the expected result of future research. SRAM cells require special attention when considering memory optimization. The development of alternative designs of SRAM memory cells will be necessary for the stability of

the same, taking into account the surface occupancy and reliable performance. Therefore, the development of robust analysis techniques of SRAM cells is also one direction of future research. Furthermore, results are expected related to multi-core architecture systems, where special attention is paid to the reliability of memory cells.

The reviewed designs combine low power circuit techniques and hardware support for typical wireless sensor network assignment. Designers can choose to optimize technology scaling to provide more performance for less active energy consumption, but in that case an increase in leakage current will need to be addressed. Activity in the vicinity of the threshold voltage, rather than below it, could provide a compromise that would allow devices to require less energy with the leakage energy minimized. With more research effort, in the future wireless sensor networks can be made up of ultra-low power nodes that offer high power computation and can be deployed for a long time.

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