

# FPGA Implementation of Demodulators in Software Defined Radio Systems

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**Abstract**—The implementation of digital demodulators using FPGA platform has been presented in this paper. The software-hardware platform based on Spartan 3A has been developed for digital signal processing purposes. This platform represents the optimal choice from the standpoint of costs, performance and power consumption. The bank of FIR filters is particularly designed for signal analysis applications. AM and FM demodulators are developed and implemented on this platform. Results of practical realization of demodulators are given.

**Keywords**-Digital demodulator; FPGA; Software defined radio; Spartan 3A; AM demodulation; FM demodulation; FIR filters;

## I. INTRODUCTION

Software defined radio replaced the traditional approach to the design of wireless systems. Greater flexibility is reflected in possibility to use the same hardware for different systems. Blocks in radio system are replaced by software modules implemented on suitable hardware platform. Demodulators are the vital parts of any receiver system. Up to the last decade, era of analog demodulators was dominant. Hardware complexity of system and low flexibility were enormous obstacles. Rapid development of digital electronics set the milestone for era of digital signal processing. Digital demodulators emerged as a natural solution that offers high flexibility and efficiency. These demodulators are commonly referred as software defined demodulators. Software defined radio concept is based on philosophy of implementing different functions of signal processing on the same hardware [1], [2]. Advantages of software defined demodulators in regard to its analog counterparts are numerous: higher flexibility, configurability, lower price, lower complexity etc. In the first phase, demodulators were implemented digitally by means of digital signal processors. Sequential nature of this type of processing imposed setback in applications with very demanding computing. In second phase, the solution for this problem emerged in the form of field programmable gate arrays (FPGAs). FPGAs have very wide implementation of signal processing functions at physical layer in software defined radio systems. They are based on custom hardware architecture of high performance. All processing and computing is performed in parallel fashion instead of sequential way. Therefore, the computing using the intense signal processing could be performed.

## II. DEMODULATOR BLOCK

Demodulator block provides the selection of signals at wanted frequency and its demodulation. Demodulator's module consists of: block for translation to the IF (Intermediate Frequency), block for AGC (automatic gain control) and block for digital signal processing. After signal is down-converted to the intermediate frequency, digitalization of signal is performed. Algorithm of automatic gain control is applied to the digitized signal. Then, digital signal processing in baseband is performed. Architecture of block for digital signal processing is based on building blocks such as: bank of FIR (Finite Impulse Response) filters and bank of demodulators. Bank of FIR filters consists of FIR filters of different widths in order to accommodate bandwidths of various modulated signals. Also, functions such as generation of output audio signal and generation of digitized IQ components at the output are provided. Architecture of demodulator block is shown in Figure 1.



Figure 1. General block diagram of demodulator block

Block for automatic gain control is very important, because its function is to provide appropriate signal level for further processing. It is based on digital phased locked loop. Using the feedback, this block tries to minimize signal error.

There are also some important subsystems that communicate with demodulator. Microprocessor is needed in order to set parameters of demodulator. This is the block that provides communication with the FPGA (demodulator) and with outside world. Also, it should be mentioned that very often, there is a need for signal shifting up and/or down in frequency. For this purpose, DDC/DUC (Digital Down converter/Digital Up converter) implemented in FPGA are used. From the stand point of demodulator, digital down converter could be very useful to facilitate further signal processing.

### III. SOFTWARE-HARDWARE FPGA PLATFORM BASED ON SPARTAN 3A

Software-hardware FPGA platform based on Spartan 3A for purpose of digital signal processing in various systems of software defined radio is developed. It provides very flexible and efficient signal processing in digital domain. Platform is fully designed in semiconductor technology. Communication with platform is realized via USB and RS232 interface. FPGA chip used on this platform is Spartan 3A DSP 3400 [3]. This platform is generic FPGA platform with computing power and memory resources needed for very fast and complex algorithms applied to signal processing in IF band. Also, analog-to-digital and digital-to-analog converters are mounted on the board. Analog-to-digital converter has resolution of 14-bit with 125MSPS, therefore according to Nyquist theorem, digitalization up to 50MHz is available. Digital-to-analog converter has resolution of 14-bit with 125MSPS, also according to Nyquist theorem, reconstruction of analog signal up to 50MHz is available. In this way, the complete system for digital signal processing is provided. Fast communication with main computer system is provided by means of PCI bus. Large number of input/output control lines is available, which provides great flexibility of working in different environments. Control of FPGA chip and communication with outside world is realized by general purpose processor. Architecture of developed software-hardware FPGA platform is shown in Figure 2.

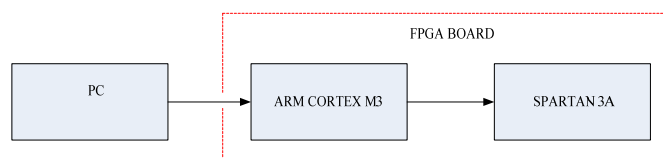


Figure 2. Architecture of FPGA board

Spartan 3A DSP is modern FPGA chip that represents optimal compromise between costs, performance and power consumption. It is very convenient for implementation in the devices in low and medium series. This chip is last generation in 90nm technology with largest number of Xtreme DSP48A blocks for performing MAC (Multiply-accumulate) operations and largest memory resources in complete Spartan 3 family. Two key modules for digital signal processing, Xtreme DSP48A blocks and RAM blocks work up to 250MHz. This architecture based on dedicated hardware lines and parallel processing gives potential for designing ultra-fast filters for extremely demanding digital signal processing applications. Hence, Spartan 3A represents logical solution of high performances and low costs, intended for wide spectrum of applications.

Control of Spartan 3A chip and setting of its parameters is performed by means of microprocessor. For this purpose ARM CORTEX M3 processor is selected. The processor uses the system clock at 72 MHz.

The implemented FPGA platform based on Spartan 3 is programmed by loading configuration data into robust, reprogrammable, static CMOS configuration latches that collectively control all functional elements and routing resources. The detailed architecture of developed software-hardware FPGA platform is shown in Figure 3.

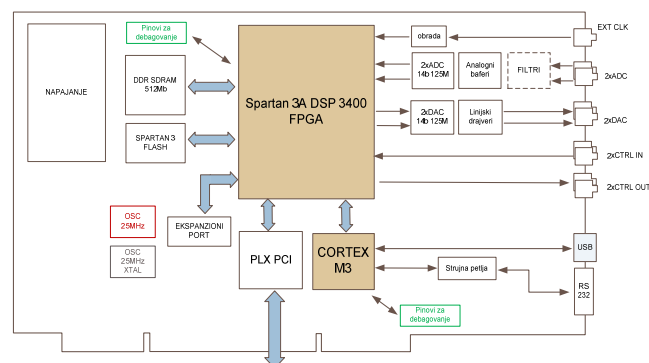


Figure 3. Detailed architecture of FPGA board

Fabrication of developed FPGA board is realized in eight layers surface mounted devices (SMD) technology. Physical assembly of FPGA board is shown in Figure 4.

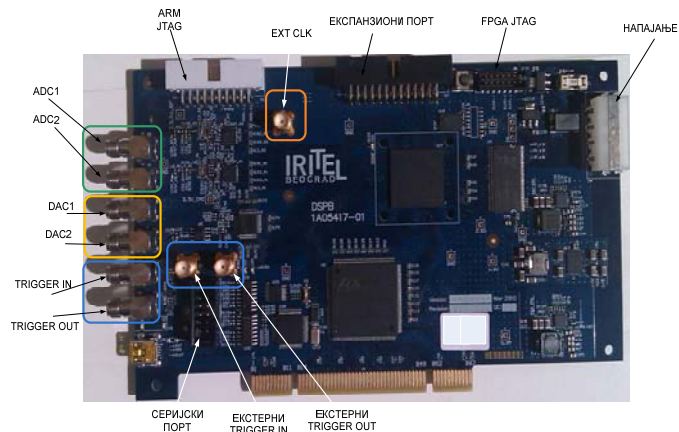


Figure 4. Physical assembly of FPGA board

This board uses internal clock, but external clocking is also available. Power supply of the board is provided by means of 4-pin peripheral connector. Power supply voltage is +5 V. Current consumption under heavy load is up to 1,5 A. Board can operate stand alone or to be plugged into the mother board of the PC. Two SMA connectors for analog-to-digital conversion are available. In addition, two SMA connectors for digital-to-analog converters are provided. For debugging purposes, JTAG (Joint Test Action Group) port is available. JTAG port is also used to download bistream to the FPGA chip. If there is a need for connecting more than one platform, expansion port can be used. For communication purposes, USB and RS-232 connectors are mounted on the FPGA board. Hence, this board represents flexible software and hardware solution of high performance suitable for various applications.

Overview of important attributes of Spartan 3A chip mounted on the board is shown in Table 1.

TABLE I. ATTRIBUTES OF SPARTAN 3A DSP

Chip designation	DSP48A	Number of slices	System Gates	Equivalent logic cells
Spartan 3A 3400	126	23872	3400000	53712

The most important characteristics of Spartan 3A 3400 chip are depicted in this table. Also, it should be mentioned that capacity of block RAM is 2268 KB. The number of CLB (*Configurable Logic Block*) is 5968. It could be worth emphasizing that there is 23872 slices. All these numbers represent high performance and flexibility. Thus, this chip can be used for very demanding applications where intense digital signal processing is needed.

#### IV. MEASUREMENTS RESULTS

First step in the design of software defined demodulator is to create the model in MATLAB/SIMULINK [4]. This is the basis for configurable computing in SDR systems. Xilinx System Generator in MATLAB is used as the complete system model. This is a system level tool for modeling and testing [5]. In this way, the exact FPGA implementation is achieved. System Generator is used for complete simulation and testing of the demodulators design flow.

The complete model of demodulator created in SIMULINK is shown in Figure 5.

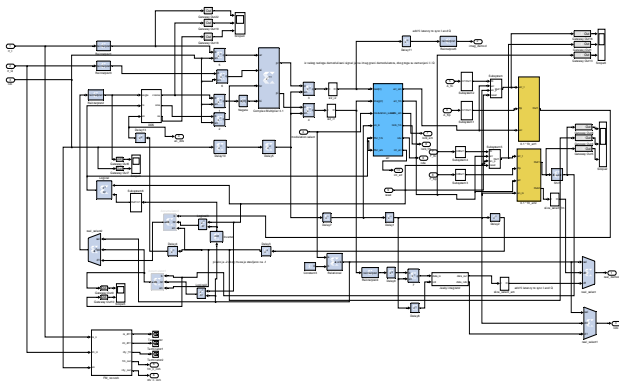


Figure 5. Complete model of demodulator

SIMULINK with System Generator is visual data flow environment where designing and testing DSP systems for FPGA platforms is provided. The *System Generator* based design flow [6] is shown in Figure 6. The system model is created in MATLAB environment using Xilinx library. All steps, from SIMULINK model to the bit stream generation are clearly depicted in design flow in Figure 6.

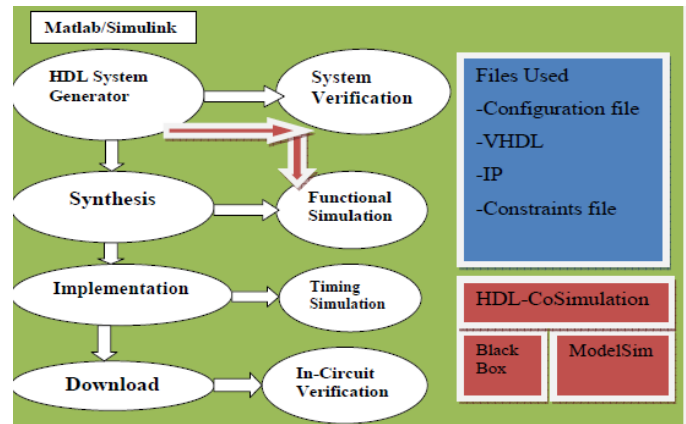


Figure 6. System Generator based design flow (Xilinx Inc., 2003)

The confirmation of the created model is performed through simulations. Results of measurements are shown in figures 7-10.

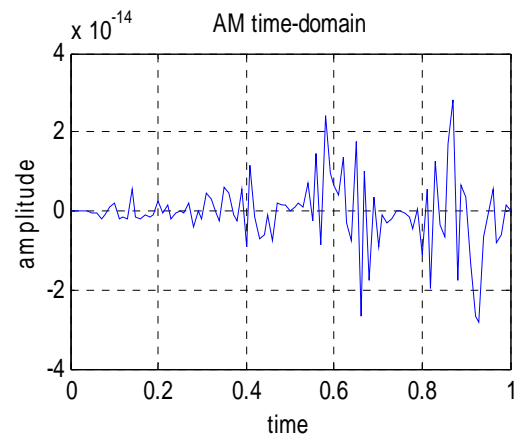


Figure 7. AM modulated signal in time-domain

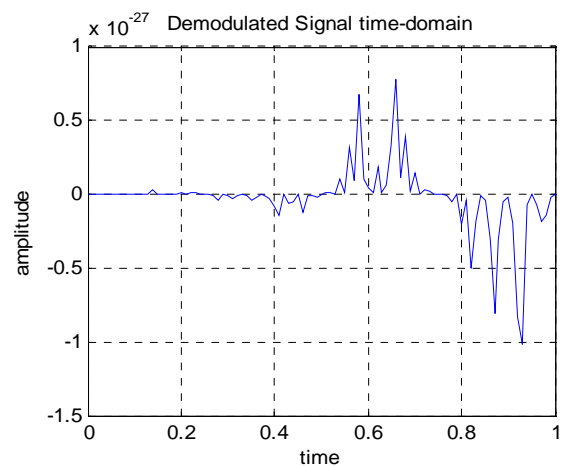


Figure 8. Demodulated AM signal in time-domain

## V. CONCLUSION

The development and design of software defined demodulators is presented in this paper. FPGA implementation was the main design requirement. In the first step, general architecture of software defined demodulator is described. It consists of block for automatic gain control, bank of FIR filters and bank of demodulators. For the purpose of digital signal processing in SDR systems, software-hardware FPGA platform has been developed. Platform is based on Xilinx Spartan 3A DSP 3400 chip. This platform represents optimal compromise between costs, performance and power consumption. Overall system analysis has been performed in SIMULINK. Two types of demodulators are designed, AM demodulator and FM demodulator. The results of practical realization of AM and FM demodulators are obtained and shown. Further research will be concerned with HF radio and VHF/UHF radio applications within the scope of software defined radio design.

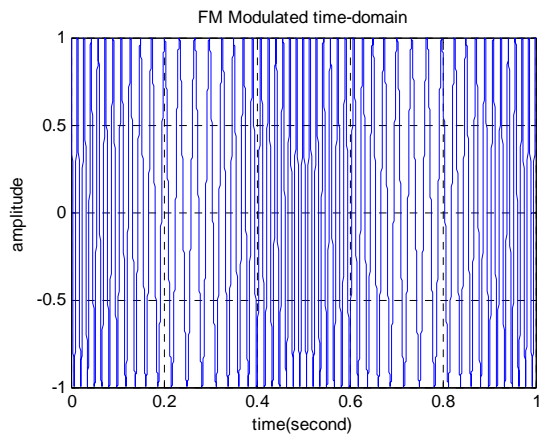


Figure 9. FM modulated signal in time-domain

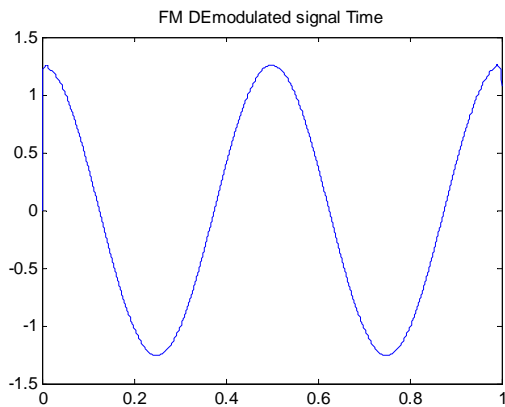


Figure 10. Demodulated FM signal in time-domain

As it can be seen from figures 7-10, modulated AM and FM signals are depicted with their demodulated counterparts.

## ACKNOWLEDGMENT

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