DESIGN AND IMPLEMENTATION OF AN EMBEDDED MICROCOMPUTER SYSTEM FOR POWER FACTOR CORRECTION

Kosta Karpuzovski, Josif Kosev, *Department for Electronics, Faculty of Electrical Engineering and Information Technologies, University Ss. Cyril and Methodius, Skopje, Macedonia*

Abstract— This study deals with the design and improvement of a power factor correction (PFC) system. Existing solutions are investigated, algorithms compared in complexities they impose on microcontrollers in static and dynamic mode, along with the advantages of digital versus analog solutions. Boost Converter will be used as a reference PFC system.

1. INTRODUCTION

Embedded microcomputer systems designed for closed loop control implementations are extensively used in areas of motor control, uninterruptible power supplies (UPS), switching mode power supply (SMPS), and motion control applications. Typical low to medium power implementations of these systems have power supplies consisting of uncontrolled bridge rectifier and capacitor filter. They impose narrow current pulses into the utility that contain significant amount of harmonics. This is polluting the utility [1] and reducing the input power factor out of the range specified in the international regulations [2, 3]. It also reduces the power efficiency of the system. Obtaining nearly ideal resistive characteristic of the load at the utility line connection, low harmonic current injection into the line and high power efficiency of the system nowadays is a must for every system designer. Therefore it is necessary to include a front end for power factor correction in every power supply system design.

There are various types of single phase PFC converters [4]. An investigation of the different types of PFC system topologies reveals that the most popular topology for PFC converter is the boost converter. It has continuous input current that can be controlled using various control algorithms to force it to follow the changes of the input voltage and thus making the system appear to the utility as purely resistive. Therefore it will be the target system for the design in this work.

Taking boost converter as reference design, the resources it imposes on the system, such as A/D converters (with definitions of minimal sampling rate and sampling resolution), PWM outputs (with optimal output frequency and PWM resolution) and microprocessor bandwidth (over algorithm complexity and memory requirements) will be investigated and minimization methods will be proposed. Considering the new generation of peripheral-rich DSP controllers, the possibility to include both - the primary system (SMPS, UPS) and the PFC control - in one microcontroller will be considered, to make it even more cost effective. The cost-aware design is always the goal in industry and nowadays more often in academic research too.

2. ANALOG AND DIGITAL CONTROL

2.1 Analog control

Traditionally, the analog control model is the first choice for designing the system for PFC, known as analog-PFC. There are many integrated circuits available for analog-PFC. It is simple and fast to implement because the control algorithm and the performances of the system are predefined by the manufacturer [5]. Analog-PFC IC's provide improved power factor by continuous processing of the signal and have very high bandwidth. Analog processing also implies infinite resolution of the signal that is measured (down to the noise level). On the other hand analog-PFC systems have some strong drawbacks. High part count, susceptibility to aging and environment variations, along with the fixed control algorithm, are making them less attractive for new designs of PFC systems.

2.2 Digital control

Digital control for PFC gains in popularity, considering the ever increasing computing power, peripheral richness and low cost of digital signal controllers (DSCs).

Compared to traditional analog control, digital control systems provide many distinctive advantages:

- standard control hardware design for multiple platforms
- programmability
- low component count
- no susceptibility to aging and environmental variations
- better noise immunity
- ease of implementations of sophisticated control algorithms
- flexible design modifications to meet a specific customer need
- single chip solution for both control and communication functions
- possibilities for single chip solution of the complete system

Digital control also decreases the physical volume of the system transferring the control algorithm complexities in software implementation. Therefore the main focus of this work is on digital control solutions, their implementation, and possible improvements.

Digital control in PFC systems brings many pertinent factors that need to be addressed in the design and implementation of the digital control loop. Redefinition of the analog control blocks and the associated parameters in digital domain are essential for the analog designers to change the control design from the analog hardware to its digital and software counterpart. This paper discusses different implementation aspects of the average current mode control for a power factor correction (PFC) system.

3. SINGLE-PHASE BOOST PFC CONVERTER

The single-phase boost PFC converter incorporates an input diode bridge rectifier, PFC inductance L, PFC diode D, PFC switch T and DC bus capacitor C (Figure 1). The input current is controlled using the PFC switch to achieve the desired input current and the desired level for the DC bus voltage.

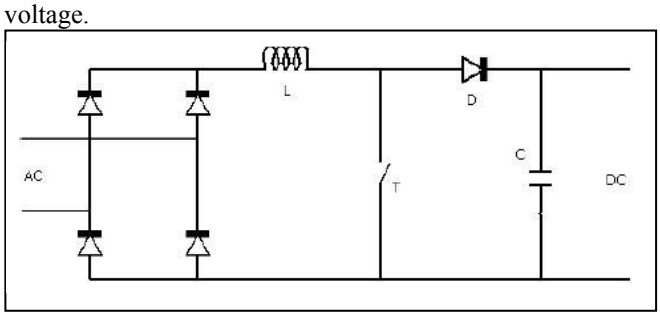

Figure 1. Single-Phase Boost PFC Converter Topology

3.1. Input requirements for PFC system

To implement digital control on a basically continuous system, we need an ADC with appropriate sample-and-hold circuits and a digital-to-analog converter (PWM in our case) for digital and analog signal interfaces. Because the ADC and PWM quantize signals, the speed and the resolution of ADC and PWM may be critical requirements in this application. In analog control the compensator is designed with operational amplifiers, while the control law in digital control system is executed by binary calculation. This introduces inevitable delay in the control system which depends on the speed of the digital controller. The presence of a signal of frequency higher than half of the sampling frequency can affect the controller by the aliasing effect. This forces the requirements for input low pass filtering and/or selecting a higher sampling frequency [6].

1) Resolution of ADC and PWM: In digital control continuous signals are converted into discrete signals at the input of the controller, while the controller output is converted back into a continuous signal that is the duty cycle of the gate-drive signal for the switch-mode power converter. This process of quantization at the input and also at the output introduces disturbances and noise into the control system and can produce undesired oscillations or distortion of the current waveform.

Since the harmonics produced by quantization should not exceed the maximum permissible harmonic standard, we need to determine the resolution requirements for the ADC and PWM.

In a PFC circuit, three signals are sampled: inductor current, input voltage and output voltage. Since the bandwidths of the signals are different, so are the sampling rate and resolution requirements. It is also necessary to pay attention to the range of the sampled signal.

The input current in PFC converter tracks the input voltage. To guarantee a high power factor, the ADC resolution must be high enough to reduce the sensing noise.

To determine the exact value of ADC resolution we can use the expression (1). It is a simplified form of border case for the relationship between input current and noise at low frequencies [6],

$$\frac{R}{2}\cdot\frac{4}{\pi}\cdot\frac{1}{K_i}\le 0.046\sqrt{2} \qquad (1)$$

where R is quantization step and Ki is current sensor gain. The minimal value for maximal allowed harmonic content in the input current is defined for 40th harmonic with absolute value of 0.046A (defined by the requirements of IEC 61000-3-2 Class A). For typical value of Ki = 0.0725, the quantization step should be smaller then 0.74%. This is equivalent to 8-bit resolution.

The input voltage is sampled for two purposes: giving the shape of the current reference and as input of the feed-forward low-pass filter.

ADC is required to have precision of at least 99.9% of PF reference to stay in the limits of allowed harmonic content in the current it sources from the utility. This, along with the voltage range of the input voltage imposes minimal resolution of ADC.

In a typical case of input voltages in the range between 90 and 240V it imposes a resolution of 8 bits.

Output voltage ADC is defined by precision we want to have when regulating it and the absolute value we regulate.

For 1% precision and 400V value of the output voltage we need an ADC with 7 bit resolution.

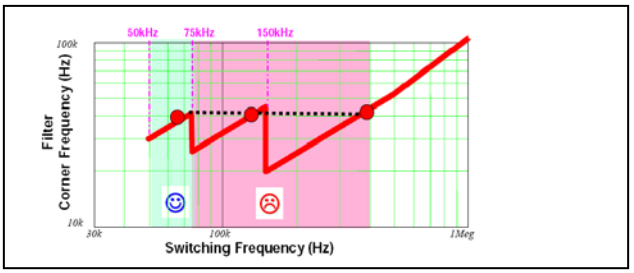

Figure 2. Relationship between EMI filter corner frequency and PWM switching frequency (Fig. 1.20 [7])

When defining the sampling frequency for the current loop we have to consider that it is directly dependable on switching frequency of the PWM. For this reason we will define the PWM switching frequency first. When defining the PWM switching frequency we have to consider several factors like PFC inductor size (its size decreases with frequency increase), system clock (system clock frequency increases with increased frequency and resolution of PWM) and EMI filter size. The EMI filter, however, is difficult to

reduce and can take up to 23% of the total front-end converter size in today's state-of-the-art power supply design. Existing studies show that the EMI filter may not be reduced by increasing the switching frequency, as shown in Fig. 2. Choosing the PFC switching frequency to be 65 kHz, 130 kHz, and 400 kHz, the EMI filter sizes are essentially the same. In another word, increasing switching frequency is not an effective way to reduce the EMI filter size. The EMI filter actually runs into a big penalty in terms of size when the switching frequency is higher than 150 kHz, unless it can be operated higher than 400 kHz [7].

Taking the above in consideration the sampling frequency for current loop is designed to be 65 kHz, which is well above the current loop bandwidth (2~10kHz). The sampling frequency is the same as the switching frequency. It is costly to have high frequency ADC. The best way to avoid the aliasing effect is to insert low-pass filter before the ADC, which can filter out the switching noise Fig. 3.

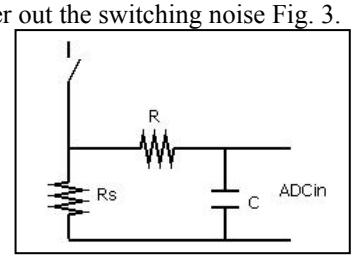

Figure 3. Low pass filter for the switching noise

For the feed-forward low-pass filter, although the bandwidth is very low, the existence of high order harmonic can still cause the aliasing effect. Furthermore, since the input voltage waveform serves as the current reference waveform; higher-order harmonics should be preserved [6]. Therefore, the input voltage sampling frequency should be high enough to avoid these high order harmonic components being wrapped into low frequencies. Having this entire set of requirements in mind we choose sampling frequency of 65 kHz.

Digital PWM resolution is closely related to the system clock. For a typical digital signal controller PWM operation is based on the system clock. For a given switching frequency, the higher is the specified resolution, the higher must be the system clock, which increases the system cost.

To determine the exact value of PWM resolution we can use the expression (2). It is a simplified form of border case for the relationship between PWM error ω and input current harmonics content at low frequencies [6],

$$\left|\omega \frac{G_{id}}{1+T_c}\right| \le 0.046\sqrt{2} \qquad (2)$$

where ω is PWM error, Gid is duty-to-current transfer function and Tc is current open loop gain. The minimal value for maximal allowed harmonic content in the input current is defined for 40th harmonic with absolute value of 0.046 A (defined by the requirements of IEC 61000-3-2 Class A). This expression can be further optimized to

$$|\omega|_{\max}\left|\frac{G_{id}}{1+CG_{id}K_i}\right|_{\max} \approx \left|\frac{R}{2}\cdot\frac{4}{\pi}\right|\left|\frac{2\pi f_{40th}}{\omega_i K_i}\right| \le 0.046\sqrt{2} \quad (3)$$

where C(s) is the current compensator transfer function, R is quantization step and Ki is current sensor gain. For typical value of L=380uH, Vout = 400V and crossover frequency fc = 8kHz, the quantization step should be smaller then 1.08%. This is equivalent to 7-bit resolution. It is safe to choose 8-bit resolution to stay in the set limits for digital current compensator implementation.

Although digital control is different from analog control, the frequency responses of the digital and the analog controlled systems are similar within the frequency range specified in IEC61000-3-2. This is far below the current loop crossover frequency. For convenience, analog compensator is used to represent the digital compensator and related delays.

2) Digital Delay: The sample and hold of continuous signals and the non-zero computation time cause delay in a digital control system. Delay in a system usually causes phase lag that leads to reduction of the phase margin.

The fastest loop in a PFC converter is the current loop, so the digital delay mostly affects the current loop. Assuming that the current loop control algorithm is executed with 8kHz rate and the controller has one switching cycle or 10us delay for ADC, PWM and computation, there is 29o phase shift in the control loop reducing the phase margin by the same value. This delay has to be compensated to stabilize the system. It is predictable that compensating this delay will result in a poor current compensator performance.

3.2. Designing the physical elements of the system

When designing the system, values for PFC inductance, output capacitance, PFC diode and the characteristics of the switching element must be calculated.

The required inductance value can be calculated using the expression [9]

$$L = \frac{\sqrt{2}\cdot V_{in}\cdot D}{fs\cdot \Delta_i} \qquad (4)$$

where Vin is input voltage RMS value, D is duty cycle, fc is switching frequency and Δi is inductance current ripple. To design the PFC switch we must choose the suitable reverse voltage, considering input and output voltages. The conduction resistance rds(on) must be as low as possible to minimize the losses while maximal rated current can be determined from the expression [9]

$$I_p = \frac{D_{\max}}{\eta}\cdot\frac{P_{out}/2}{V_{\min(REC)}} \qquad (5)$$

where Ip is the maximal current in the switching element, Dmax is the maximal duty cycle, η is the converter efficiency, Pout is the nominal output power and Vmin(REC) is the RMS value of the minimal rectified voltage.

When designing the PFC diode we must consider reverse voltage, forward current and switching speed. Forward current can be approximated with the peak current of the switching element.

The DC bus capacitance needs to comply with voltage requirements of the output voltage we defined and ripple constraints in one switching cycle.

3.3. Designing the Digital Control of the PFC system

The requirement on the resolution of ADC, PWM and system clock is summarized in Table 1. Due to the fact that ADC and PWM are built-in peripherals in the DSC, most restricting requirements should be considered when selecting the appropriate component. For the typical design discussed above the sampling rate for the ADC module is set at 65 kHz, with resolution of at least 8 bits. PWM module should be selected with switching frequency higher than 65 kHz and resolution of at least 8 bits.

TABLE I. SUMMARY ON DIGITAL CONTROL PERIPHERIAL REQUIREMENT

Peripheral name	*Requirement*
System clock (MHz)	16
ADC channels (n)	3
ADC resolution (Bit)	8
PWM channels (n)	1
PWM resolution (Bit)	8

Using the analysis above and the requirements set on the peripherals it is possible to start the design of a digitally controlled APFC system.

Freescale MC56F8037 was chosen for the PFC implementation. Instead of focusing on traditional PFC for motor control it was decided to make the implementation on a traditional low voltage power supply. The design contains one transformer of 2x12V and a PFC to both correct power factor and provide stabilized output voltage of 20V. In this design the transformer provides both low voltage AC supply and acts as a EMI filter for high order harmonics. This solution was decided due to the fact that most of the nowadays designs are already having microcontrollers which opens the possibility to employ it in PFC while doing other functions it was designed for.

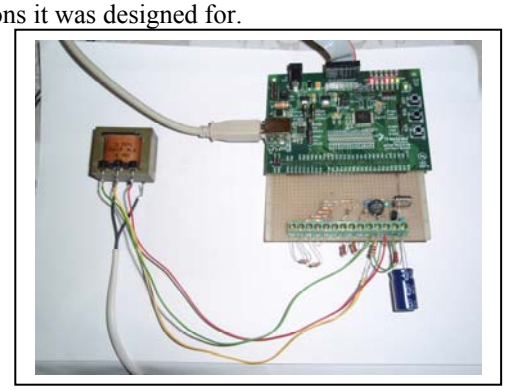

Figure 4. Implementation with MC56F8037EVB

The function of the PFC converter is dual: to control the input current towards ideal input power factor, and at the same time to provide the required stable DC bus voltage for the load. To obtain both: excellent steady-state and dynamic-state performance, it is recommended to use the control scheme of an outer-loop DC bus voltage control and inner-loop inductance current control system.

The inner inductance-current control-loop should:

- control the system input current to closely follow the reference current
- accelerate the dynamic process by providing maximum permitted current to the output when the outer DC bus voltage loop is in a transition
- provide a timely anti-jamming function against line fluctuations

To achieve the best possible functioning of the inner inductance-current loop, PI regulator should be used. The design of the inner inductance current loop is the most critical step when optimizing the PFC system. It has the most severe time constraints and also highest impact on the input current harmonic contents. Solutions in the literature propose a type I control system (PI regulator with 1 pole on the origin) [9], two-zero design [6] or fuzzy logic control algorithm [10]. The solutions try to achieve better performance, lower contents of harmonic components in input current, and lower computational power at the same time, to reduce the system costs.

To track the input voltage according to standard limitations imposed on the input current, the bandwidth is set to 8 kHz. To improve the anti-jamming performance against line fluctuation for the inner inductance current loop, the rectified input voltage is added into the inner inductance current loop as the feed-forward control signal.

The outer DC bus voltage loop is aimed to:

- control the DC bus voltage to quickly follow the change of reference voltage and implement zero-error control in steady state
- determine the maximum permitted output current through limiting the voltage regulator output
- provide a timely anti-jamming function against the load variations

The design of outer DC bus voltage loop, although not as critical as inner current control loop is important when designing the PFC system. It has highest impact on the stability of the output voltage. Solutions in the literature include a type II control system (PI regulator with 2 poles on the origin) [9], minimal error optimization [6] and fuzzy logic control algorithm [10]. The solutions show that voltage loop bandwidth is around 6 Hz.

The proposed control system has an outer loop for DC bus voltage regulation, a feed-forward loop for the input voltage, and inner loop for inductance-current regulation for the designed PFC converter. When implementing the solution in a microcontroller, control algorithm execution time should be considered to avoid solutions where slower loops are executed once in every n cycles [6]. This introduces variable calculation time in the system control loop, adding jitter in the PWM duty cycle calculation.

Besides processing of the main control loop, the total input current should be measured, and the RMS input voltage should be calculated during the control process. This information is used to protect the power stage from over-voltage, under-voltage, and/or over-current conditions.

Taking in account the notorious problems of analog-PFC solutions, the inductor saturation and the dependency of output power on input voltage, we can design the digital PFC system to act pro-actively in these conditions.

Optimization of the implementation should be one of the most important parts of the process. Different techniques should be used for the implementation of different parts of the system. A good example is to use discrete implementation of an analog filter with two poles instead of Butterworth or Chebyshev filters. This saves computation time because of the simpler implementation. It also increases the stability of the system because the coefficients are neither too small nor sensitive [6].

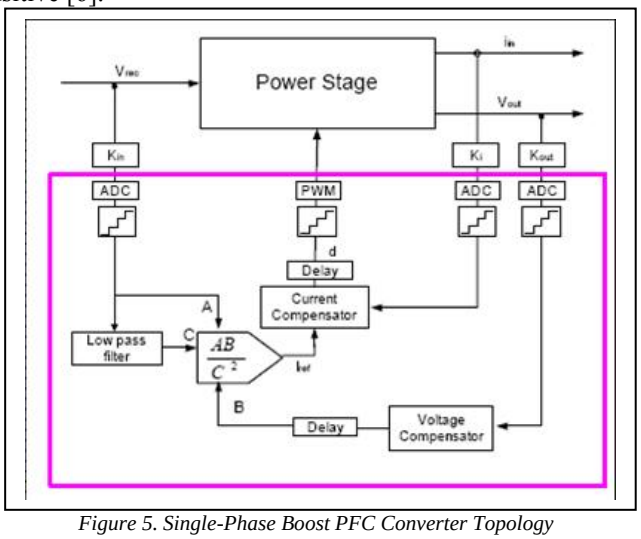

Figure 5. Single-Phase Boost PFC Converter Topology

4. CONCLUSIONS

The design of a PFC system using a Boost converter as reference design is analyzed. Aspects like power density, disturbance resistance and implementation complexities were discussed. Different implementations are shown with their advantages and disadvantages and the improvements with recent implementations. New switching components offer lower recovery time for the PFC diode and lower Rds(on) for the switching transistor. New designs, using newer technology, are lowering loses in the components, making the PFCs more efficient. Microcontrollers have more peripherals and their increased computing power opens new horizons.

In the implementation we used to test the algorithms, PI regulator provided the best performance, but the fuzzy logic control algorithm was the fastest and provides more space to implement main circuit functionalities.

General trend in the industry is getting higher power density of the devices for PFC. Good results are reported for interleaved operation, offering lower interference in the input current and smaller ripple in the output voltage. Gain is evident for as many as 4 interleaved PFCs working in parallel with controlled phase shift. Highest gain is in the size of EMI filter, which proved to be constant for switching frequencies as high as 400 kHz [7]. Interleaved operation offers better PFC efficiency at light loads.

New directions for future development are explored in using neural networks for system control or dynamic optimization of constants in the control algorithms.

Another solution for increasing the PFC efficiency, by decreasing the number of components in the current path and decreasing price by decreasing the number of components in general is the use of bridgeless PFC boost rectifier [11].

Price optimization is going one level further by reducing the sensing elements necessary to implement the control [12].

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