Performance Evaluation of New Adaptive Dual Current Mode Control of Buck Converter

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Abstract—**This paper presents experimental verification of new current control method named adaptive dual current mode control (ADCMC), which is modification of existing dual current mode control (DCMC). The given experimental results for buck converter prove the validity of the proposed ADCMC and show its important advantages over DCMC, including no peak-to-average error in the inductor current, better transient response of inner current loop and improved line regulation.**

Keywords-buck converter; current mode control (CMC); line regulation; peak-to-average error;

I. INTRODUCTION

Power electronics converters can be controlled in two main ways: voltage mode control (VMC) and current mode control (CMC). CMC has important advantages over VMC, such as overcurrent protection, better transient response (reduced order of converters' transfer function), improved line regulation by inherently built-in feed-forward property, etc. CMC is introduced in 1970s [1]. Many CMC methods have been developed since then and they have been increasingly used. CMC methods can be divided in two groups: fixed-frequency and variable-frequency methods. In literature there are many different fixed-frequency CMC methods and their modifications, including peak CMC (PCMC) [2], [3], valley CMC (VCMC) [2], [4], average CMC (ACMC) [5], [6] and charge control [7]. Among these methods, PCMC and ACMC are the most frequently used.

Although PCMC and VCMC have some excellent features, such as constant switching frequency, simple implementation and good dynamic response, they have several drawbacks. The most important one is appearance of subharmonic oscillations when the duty cycle is above 0.5 (for PCMC) or below 0.5 (for VCMC). In order to eliminate subharmonic oscillations, they need slope compensation. In [8] and [9] it is shown that PCMC and VCMC actually exhibit subharmonic oscillations even inside the above mentioned conventional stability limits, regardless of the existence of slope compensation. Exact shortened stability limits depend mostly on the outer voltage compensator.

Another important drawback of PCMC and VCMC is that they have peak-to-average error in the inductor-current. This error is defined as difference between the reference current and the average value of the inductor current over switching period. Therefore, they are not able to directly control the average value of the inductor current over switching period. This drawback is the most expressed in applications where it is important to achieve precise tracking of the reference current.

In ACMC the inductor current is scaled and filtered with low-pass filter for attenuation of high-frequency switching harmonics and fed into a current compensator. In this way the average value of the inductor current is directly controlled. ACMC provides stable operation of power converters for the entire range of duty cycle from 0 to 1 and it has improvements in noise immunity. However, due to the existence of low-pass filter in the inner current loop, its dynamic response is slower.

Variable-frequency CMC methods solve the issues of subharmonic oscillations by operating in free-running mode. One of the most popular variable-frequency methods is hysteresis CMC (HCMC) [10], [11]. It has several advantages, including no slope compensation, no subharmonic oscillations and no peak-to-average error. However, HCMC is not always practicable due to its variable frequency. There are some modifications of HCMC, as it is proposed in [12], [13], which rely on fixed-frequency operation, but with more complex implementation.

In [14] a fixed-frequency dual current mode control (DCMC) is proposed, which has two boundaries (peak and valley) for the inductor current and two clock signals phase shifted for 180 degrees. In this way DCMC naturally switches from PCMC (duty cycle bellow 0.5) to VCMC (duty cycle above 0.5) and vice versa, which ensures stable operation of power converters for the entire range of duty cycle from 0 to 1. DCMC offers important qualities, including no slope compensation and fixed-frequency operation, which make DCMC applicable in wide range of converters (DC-DC, AC-DC and DC-AC) including power factor correction (PFC) and inverter circuits. However, DCMC has one important drawback. A constant width between two current boundaries must be chosen in advance properly to be larger or equal than the maximum peak-to-peak ripple of the inductor current, causing the existence of peak-to-average current error. This can adversely affect the waveform of converter's inductor current, especially in PFC and inverter circuits, where peak-to-peak current ripple changes over fundamental period.

A new adaptive dual current mode control (ADCMC), which improves the qualities of DCMC by introducing an adaptive width between two current boundaries, which is equal to the instantaneous value of peak-to-peak current ripple over each switching period, is proposed in [15]. The aim was to obtain a new CMC method which combines all the qualities of DCMC, such as fixed-frequency, no slope compensation and stable operation of power converters for the entire range of duty cycle, with qualities of HCMC, such as no peak-to-average current error and excellent dynamical behavior. Therefore, the ADCMC is close to HCMC, but with fixed-frequency. In [15] basic principles of operation, small-signal modeling and analysis of new ADCMC method are presented, with simulation verification. In this paper experimental validation of new ADCMC is given, with evaluation of some important performances and improvements over DCMC.

This paper is organized as follows. The basic principles of operation of ADCMC for buck converter are presented in Section II. Section III presents the experimental results. The conclusion is given in Section IV.

II. BASIC PRINCIPLES OF OPERATION OF ADCMC

The basic principles of operation of DCMC proposed in [14] and its characteristic operating modes for buck converter are presented in Fig. 1. The output of voltage compensator $G_c(s)$, which is used for regulation of output voltage v_o, is actually the reference inductor current i_{ref}. The inductor current i_L is measured and compared with upper $i_{ref}+I_a$ and lower $i_{ref}-I_a$ boundaries ($I_a=const$). For correct and stable operation of DCMC the constant width between these two boundaries named the current gap $2I_a$ must be larger or equal than the maximum peak-to-peak ripple of the inductor current. Therefore, the current I_a must satisfy the following condition:

$$2I_a \geq K_{iL}\Delta i_{Lpp\max} = K_{iL}\frac{v_g}{4f_sL}, \qquad (1)$$

where: K_{iL} is inductor current's measuring gain and Δi_{Lppmax} is maximum peak-to-peak ripple of the inductor current for duty cycle D=0.5, v_g is input voltage, $f_s=1/T_s$ is switching frequency and L is the inductor value.

Three characteristic operating modes of DCMC are presented in Fig. 1.b. If duty cycle D is less than 0.5, DCMC behaves as PCMC with upper boundary $i_{ref}+I_a$. If duty cycle D is greater than 0.5, DCMC behaves as VCMC with lower boundary $i_{ref}-I_a$. If duty cycle D is equal to 0.5, the switch T is only controlled with the clock signals clk_A and clk_B. These operating modes guarantee the stable operation of buck converter for the entire range of duty cycle $0<D<1$.

It is obvious from Fig. 1.b that there is significant peak-to-average error in the inductor current. Therefore, DCMC isn't able to directly control the average value of the inductor current. In converters such as PFC or inverter circuits, where duty cycle and peak-to-peak current ripple change over fundamental period, this can be an important issue. If high current gap $2I_a$ is set, in these topologies a distortion in waveform of the inductor current occur in boundary case (D=0.5).

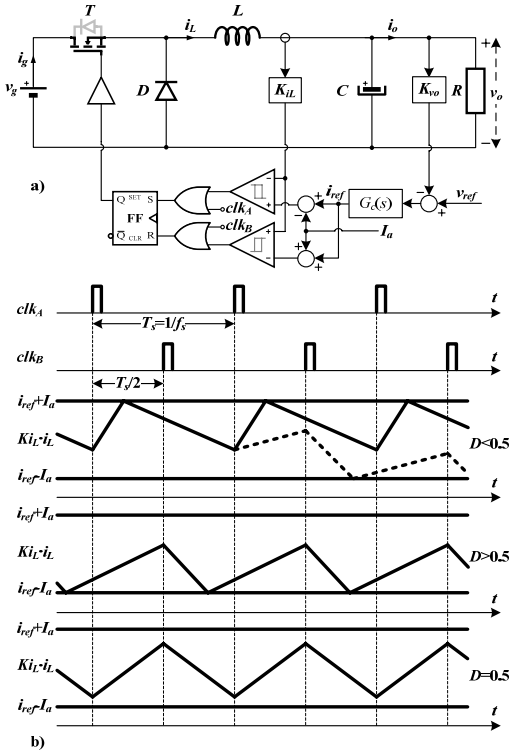

Figure 1. a) DCMC of buck converter, b) Characteristic operating modes.

In order to resolve these issues, a new ADCMC method is proposed in [15], which is based on on-line computation of adaptive current gap $2i_a$ ($i_a \neq const$), using the instantaneous value of peak-to-peak current ripple Δi_{Lpp} on each switching period T_s, in the following way:

$$2i_a = K_{ia}K_{iL}\Delta i_{Lpp}, \qquad (2)$$

where $K_{ia}\geq 1$ is scaling factor. If K_{ia}=1, the adaptive current gap $2i_a$ is equal to the instantaneous peak-to-peak current ripple $K_{iL}\Delta i_{Lpp}$. Therefore, the average value of the inductor current over each switching period is now equal to the reference current i_{ref}, giving no peak-to-average error. In this way the ADCMC becomes similar to the HCMC, but with constant switching frequency.

Equation (2) applies in general case for any type of power converter. However, due to the fact that it is very difficult to directly measure the instantaneous current ripple Δi_{Lpp}, it is calculated by measuring the input and output voltage of converter. For the buck converter from Fig. 1.a, the adaptive current gap $2i_a$ is equal to:

$$2i_a = K_{ia}K_{iL}\frac{v_o}{Lf_s}\left(1-\frac{v_o}{v_g}\right). \qquad (3)$$

It is worth to note that the control scheme of ADCMC remains the same as in Fig. 1.a. The key difference is that in ADCMC the current i_a is not predefined constant, but it is adaptive and calculated from (3). If other type of power converter is used, it is necessary to modify (3) properly according to that converter's type.

III. EXPERIMENTAL RESULTS

The setup for experimental verification of ADCMC is shown in Fig. 2. One of the key parts of this experimental setup is MF624 data acquisition digital board connected to the computer, which enables real time operation with Matlab/Simulink. The outer voltage loop for regulation of the output voltage in both DCMC and ADCMC and calculation of the adaptive current gap $2i_a$ for ADCMC are implemented in real time in Matlab/Simulink environment. The measurement circuits and inner current loop are implemented on separate electronic module which is connected to MF624 board. The inductor current is measured with LEM current transducer HX 10-NP [16] and fed into the inner current loop. The measured values of input and output voltage are brought to the analogue inputs of MF624 board and sampled by its 14-bit A/D converter. Due to the presence of measurement noise, these values are filtered in Simulink with simple averaging filter before entering in output voltage loop and calculation of the adaptive current gap $2i_a$. The reference current i_{ref} and upper and lower current boundaries are obtained from MF624 board from its 14-bit D/A converter and fed into the inner current loop on the separate electronic module. The fundamental sampling time of 25 μs was used in Simulink for real-time operation.

The prototype of power converter is designed as synchronous buck converter. The parameters of buck converter are set to ensure the continuous conduction mode (CCM) operation: V_g=28 V, L=220 μH, C=1000 μF and R=4 Ω. The maximum output power of buck converter is limited to 100 W. The switching frequency f_s is set to approximately 23 kHz. The value of I_a for DCMC was set to 1 A according to (1). The performances of ADCMC are verified with series of experiments and compared with performances of DCMC in the same operating conditions.

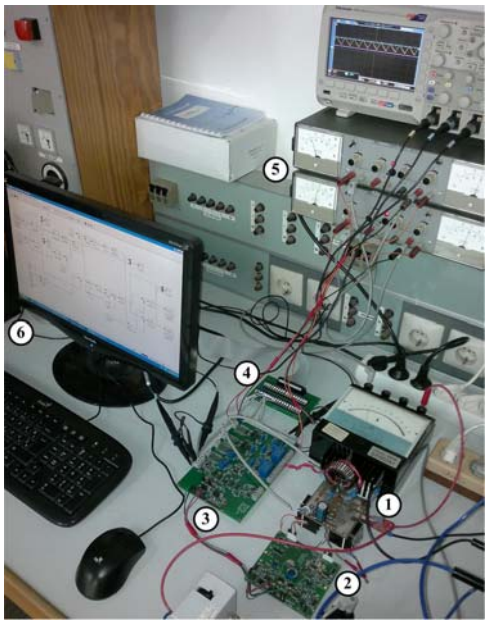

Figure 2. Experimental setup for ADCMC: 1) The prototype of synchronous buck converter; 2) MOSFET driver module; 3) Measurement circuits and electronic module for inner current loop; 4) Connectors for MF624 board; 5) Power supply units; 6) PC for real time processing with MF624 board.

A. *Peak-to-average Error in Steady State*

In order to examine peak-to-average current error for both DCMC and ADCMC, steady state was analyzed. In the first case, the outer voltage loop was disabled and the reference current i_{ref} was set as constant signal. Two values of the reference current were considered: i_{ref}=1.5 A and i_{ref}=5 A. The experimental waveforms of the inductor current, upper and lower current boundary and reference current in steady state are shown in Fig. 3 for DCMC and Fig. 4 for ADCMC.

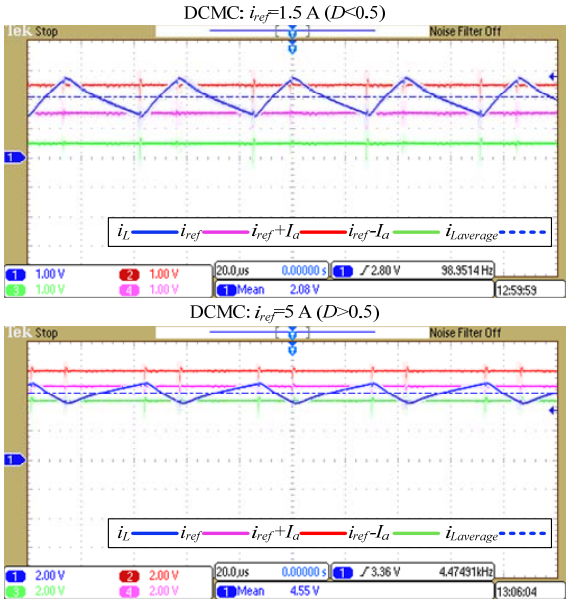

Figure 3. Experimental waveforms in steady state for DCMC without outer voltage loop.

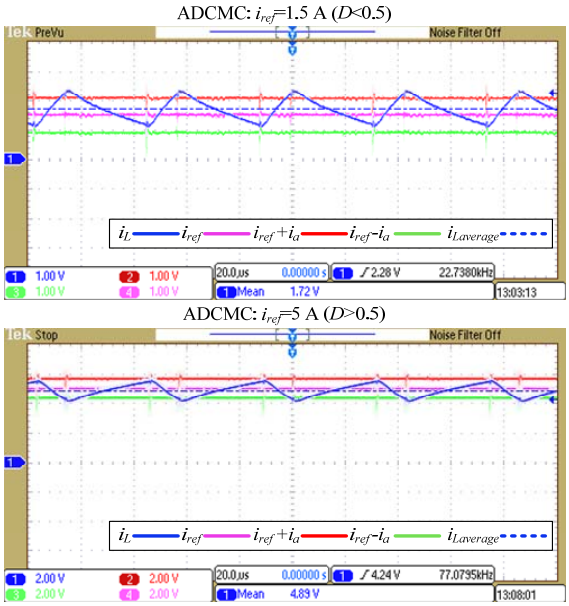

Figure 4. Experimental waveforms in steady state for ADCMC without outer voltage loop.

In the second case, the outer voltage loop was enabled. A simple proportional-integral (PI) compensator was used as the

output voltage compensator. A procedure of its design is not given, because this paper is more focused on the current control loop. Two values of the output voltage were considered: v_o=10 V and v_o=20 V. The results are shown in Fig. 5 for DCMC and Fig. 6 for ADCMC.

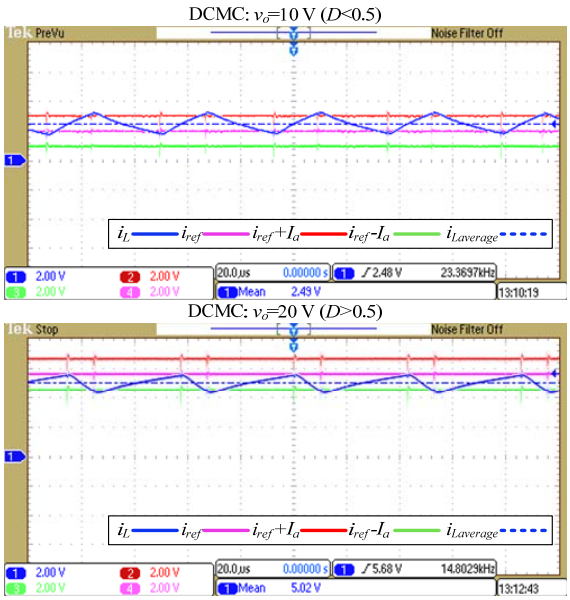

Figure 5. Experimental waveforms in steady state for DCMC with outer voltage loop.

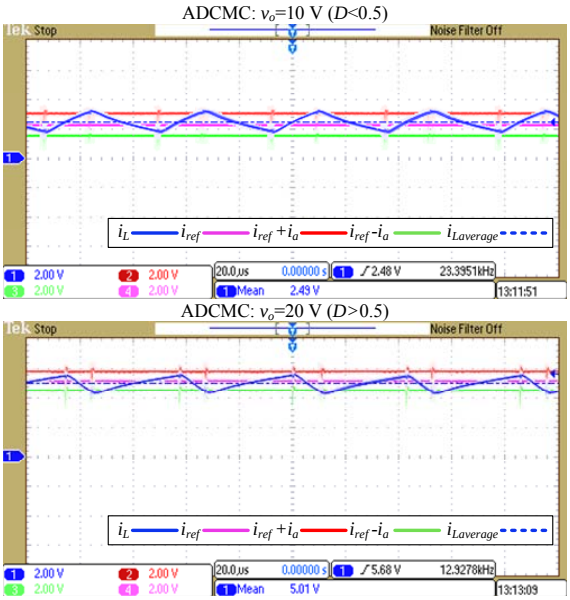

Figure 6. Experimental waveforms in steady state for ADCMC with outer voltage loop.

It is obvious from Fig. 3, Fig. 4, Fig. 5 and Fig. 6 that peak-to-average current error in steady state is much smaller for ADCMC than for DCMC. However, if noted from Fig. 4 and Fig. 6 for ADCMC, a small peak-to-average error still exists. The key reason for existence of this error is delay of comparators and MOSFET driver module. It is obvious that these delays cause the inductor current to move up (for D<0.5) or down (for D>0.5), increasing peak-to-average error. These hardware limitations should be considered in the entire development process. However, this is not the subject in this paper, but it could be interesting for analysis in future work.

B. *Line Regulation*

In order to check the line regulation performance of DCMC and ADCMC, step changes of input voltage from 28 V to 16 V and vice versa were performed in experiments, while the output voltage was regulated to the value of 10 V. The waveforms of the inductor current are shown in Fig. 7 and Fig. 8 for both DCMC and ADCMC.

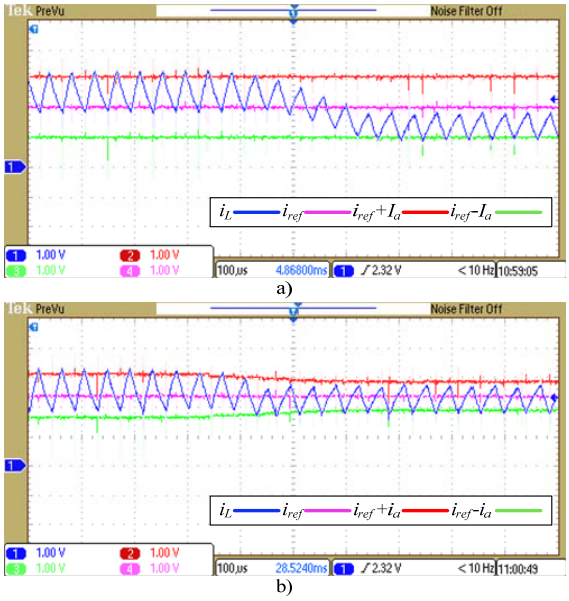

Figure 7. Experimental waveforms for a step change in the input voltage from 28 V to 16 V: a) DCMC, and b) ADCMC.

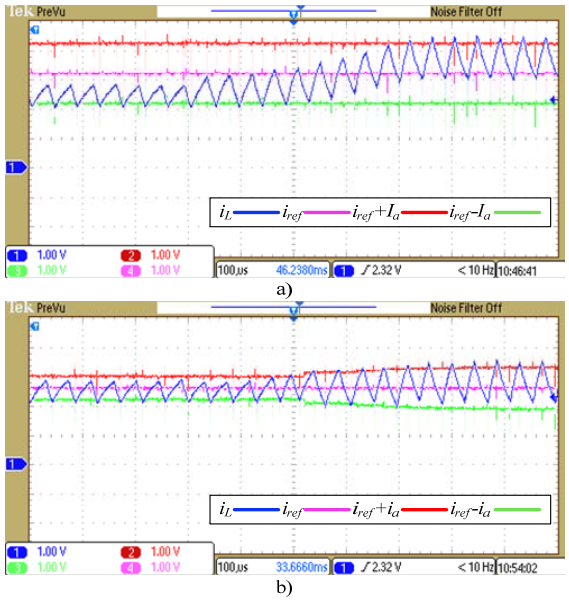

Figure 8. Experimental waveforms for a step change in the input voltage from 16 V to 28 V: a) DCMC, and b) ADCMC.

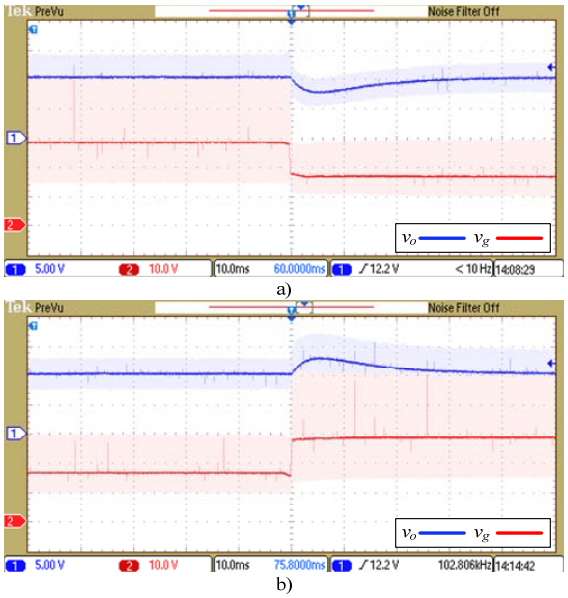

Figure 9. Experimental waveforms for a step change in the input voltage from: a) 28 V to 16 V and b): 16 V to 28 V (DCMC).

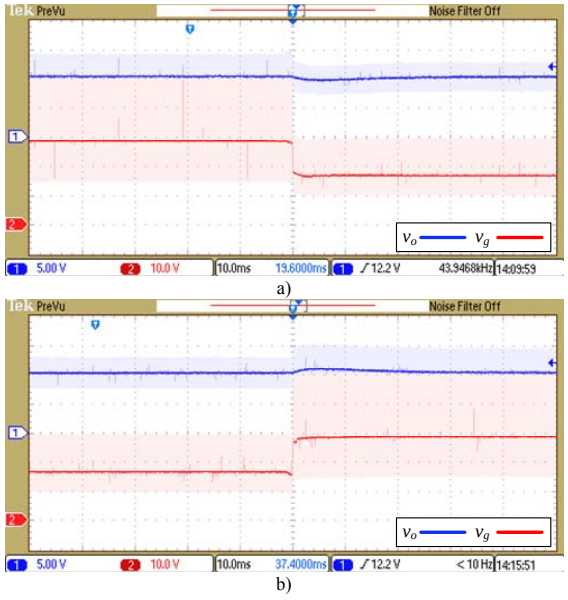

Figure 10. Experimental waveforms for a step change in the input voltage from: a) 28 V to 16 V and b): 16 V to 28 V (ADCMC).

It is obvious from Fig. 7 and Fig. 8 that ADCMC ensures better transient response of the inductor current from domain $D<0.5$ to $D>0.5$ and vice versa, which results in improved line regulation, as shown in Fig. 9 and Fig. 10.

C. *Robustness to the Load Disturbance*

Step change in the load resistance R from R=4 Ω to R=6 Ω was performed in experiments in order to verify the robustness of the proposed ADCMC to the load disturbance. The output voltage was regulated to the value of 10 V. The results are shown in Fig. 11 and Fig. 12 for both DCMC and ADCMC.

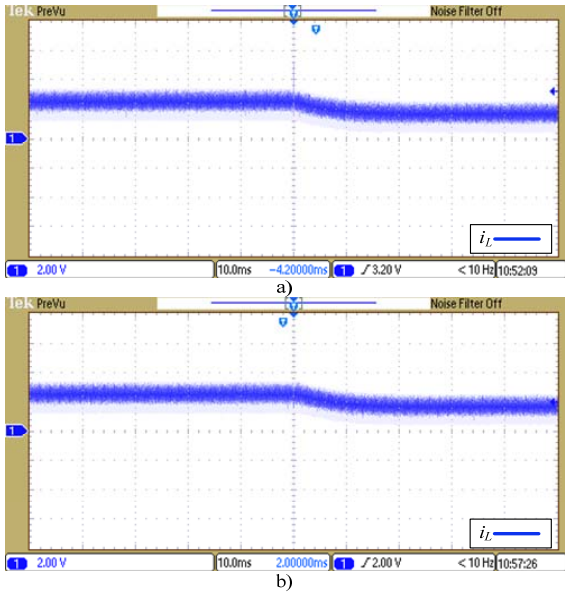

Figure 11. Inductor current for a step change in the load resistance from R=4 Ω to R=6 Ω: a) DCMC and b): ADCMC.

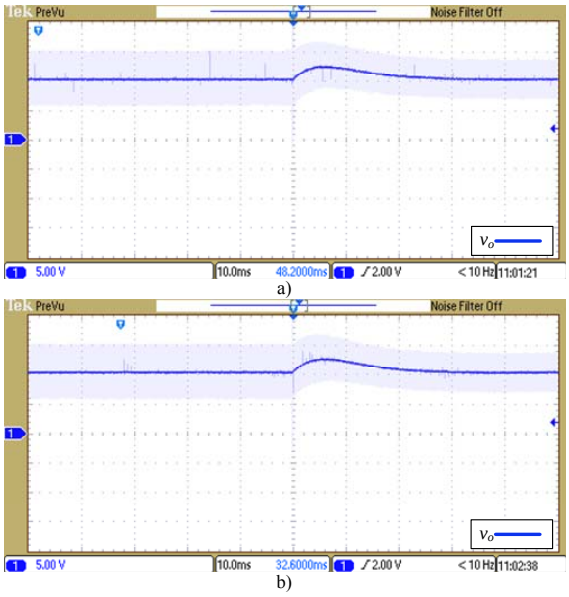

Figure 12. Output voltage for a step change in the load resistance from R=4 Ω to R=6 Ω: a) DCMC and b): ADCMC.

It is obvious from Fig. 11 and Fig. 12 that the given results are very similar for DCMC and ADCMC. Both DCMC and ADCMC successfully reject the step load disturbance.

IV. Conclusion

In this paper, a new ADCMC method was presented with experimental verification. The steady-state peak-to-average current error, line regulation and step load response have been investigated for both DCMC and the proposed new ADCMC. The experimental results showed some significant advantages of ADCMC over DCMC. There are still some issues which could be interesting for future work, including analysis of

switching delays, their impact on the ADCMC's performances and their minimization.

Another important task could be realization of adaptive current gap $2i_a$ by using the measured inductor voltage for calculation of instantaneous peak-to-peak current ripple. This makes the adaptation of current gap $2i_a$ universal and independent of converter's topology.

The next step will be implementation of the proposed ADCMC on digital platform, such as digital signal processor (DSP) and field programmable gate array (FPGA) circuit.

The most important challenge will be implementation of the proposed ADCMC on PFC and inverter, where its excellent performances would be best verified.

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